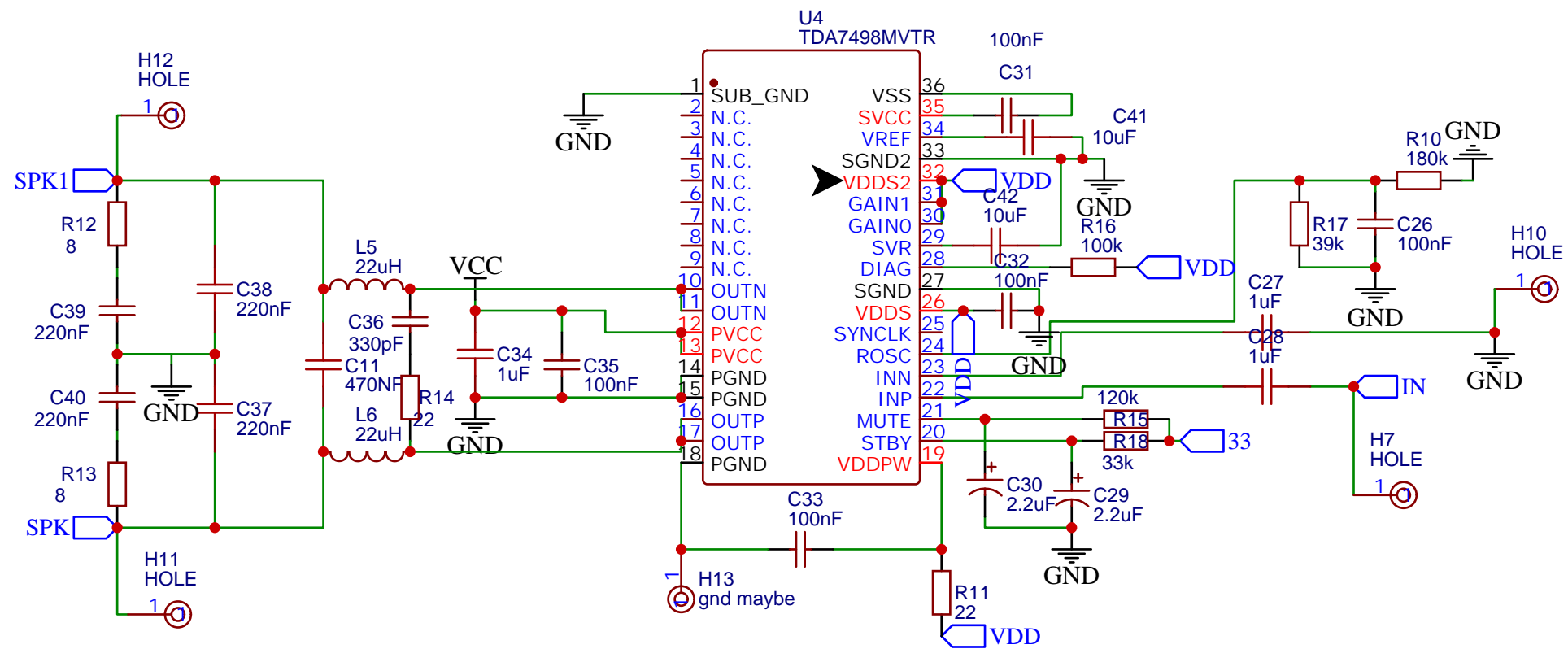


Designed:
Gain 1 and 0 set to high
mute and standby is high logic 3.3v

DIGNOSIS:
PWM OUTPUT CRO
VDDS voltage
VDDPW VOLTAGE
3.3V OUTPUT



TITLE: Sheet_1		REV: 1.0
Company: Your Company		Sheet: 1/1
Date: 2022-09-30		Drawn By: sagar saini

